	L #	Hits	Search Text	DBs	Time Stamp
1	L1	281	EDO adj (RAM or DRAM)	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:16
2	L10	195	North adj bridge	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:29
3	L11	19	1 and 10	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:33
4	L12	0	5 and 10	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:30
5	L13	16	8 and 10	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:30
6	L14	157	("711/106").CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:34

	L#	Hits	Search Text	DBs	Time Stamp
7	L15	4	1 and 14	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:35
8	L2	3407	refresn$3 same (low adj power) or (sleep adj mode)	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:23
9	L3	6	1 and 2	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:22
10	L4	0	refresh adj timing adj gererator	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:17
11	L5	29	refresh adj timing adj generator	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:18
12	L6	0	1 and 5	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:18

	L#	Hits	Search Text	DBs	Time Stamp
13	L7	0	2 and 5	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:18
14	L8	3941	refresh$3 same (low adj power) or (sleep adj mode)	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:23
15	L9	14	1 and 8	USPAT; US-PGPUB; EPO; JPO; IBM TDB	2001/10/22 14:29

	Document ID	Source	Issue Date	Pages	Title	Abstract	Current OR	Current XRef
1	US 20010010654 A1	US-PGP UB		54	Multiple ports memory-cell structure			
2	US 20010003513 A1	US-PGP UB		54	Methods to reduce the effects of leakage current for dynamic circuit elements			
3	US 6243315 B1	USPAT	20010605	67	Computer memory system with a low power down mode		365/222	365/229 ; 365/230.03 ; 365/52
4	US 6212599 B1	USPAT	20010403	16	Method and apparatus for a memory control system including a secondary controller for DRAM refresh during sleep mode		711/106	365/226 ; 365/227 ; 711/105 ; 713/1
5	US 6199134 B1	USPAT	20010306	17	Computer system with bridge logic that asserts a system management interrupt signal when an address is made to a trapped address and which also completes the cycle to the target		710/129	713/324
6	US 6134167 A	USPAT	20001017	25	Reducing power consumption in computer memory		365/222	365/229
7	US 6108229 A	USPAT	20000822	44	High performance embedded semiconductor memory device with multiple dimension first-level bit-lines		365/52	365/104 ; 365/184
8	US 6094700 A	USPAT	20000725	21	Serial bus system for sending multiple frames of unique data		710/129	710/30
9	US 6070215 A	USPAT	20000530	16	Computer system with improved transition to low power operation		710/129	713/320

	Document ID	Source	Issue Date	Pages	Title	Abstract	Current OR	Current XRef
10	US 6065122 A	USPAT	20000516	11	Smart battery power management in a computer system		713/320	710/101 ; 710/2 ; 710/260 ; 710/266 ; 713/300 ; 713/322 ; 713/323 ; 713/324 ; 713/400 ; 713/500
11	US 5881016 A	USPAT	19990309	14	Method and apparatus for optimizing power consumption and memory bandwidth in a video controller using SGRAM and SDRAM power reduction		365/230.03	365/203 ; 365/233
12	US 5859801 A	USPAT	19990112	15	Flexible fuse placement in redundant semiconductor memory		365/200	365/222 ; 365/225.7 ; 365/230.03 ; 365/230.08 ; 365/233 ; 365/240
13	US 5825704 A	USPAT	19981020	39	High performance embedded semiconductor memory devices with multiple dimension first-level bit lines		365/222	365/149 ; 365/150 ; 365/207 ; 365/230.06
14	US 5748547 A	USPAT	19980505	24	High performance semiconductor memory devices having multiple dimension bit lines		365/222	365/230.03 ; 365/63